

What is claimed is:

1. A semiconductor device comprising:
5 a semiconductor substrate;
first insulating film patterns formed on the semiconductor substrate;
a wiring formed on the first insulating film, the wiring including conductive film patterns and second insulating film patterns formed on the conductive film patterns;
third insulating film patterns formed on sidewalls of the wiring, the third insulating film
10 patterns comprising a silicon-oxide-based material; and
contact patterns formed on the wiring, wherein the contact patterns include contact spacers formed on sidewalls thereof and define contact holes that pass through the first and third insulating film patterns.
- 15 2. The semiconductor device of claim 1, wherein the third insulating film patterns are continuously formed on surfaces and sidewalls of the wiring, and the contact patterns are formed on the third insulating film patterns positioned on the wiring.
- 20 3. The semiconductor device of claim 1, wherein the third insulating film patterns are self-aligned relative to the contact spacers.
4. The semiconductor device of claim 1, wherein the contact patterns are wider than the wiring.
- 25 5. The semiconductor device of claim 1, wherein the contact pattern and the contact spacer comprise materials having etching selectivities relative to the third insulating film pattern.
6. The semiconductor device of claim 5, wherein the contact pattern and the
30 contact spacer comprise silicon nitride or polysilicon.
7. A semiconductor device comprising:
a semiconductor substrate having capacitor contact regions;
a first insulating film formed on the semiconductor substrate;

bit lines formed on the first insulating film between the capacitor contact regions, the bit lines including a conductive film pattern and an insulating film pattern formed on the conductive film pattern;

5 third insulating film patterns formed on sidewalls of the bit lines, the third insulating film including silicon oxide based material; and

contact patterns formed on the bit lines wherein the contact patterns include contact spacers formed on sidewalls thereof and define storage node contact holes that contact surfaces of the third insulating film patterns and pass through the first insulating film to expose the capacitor contact regions on the substrate between the bit lines.

10

8. The semiconductor device of claim 7, wherein the capacitor contact region comprises a landing pad electrode.

9. The semiconductor device of claim 7, wherein the third insulating film patterns
15 are continuously formed on surfaces and sidewalls of the bit lines, and the contact patterns are formed on the third insulating film patterns positioned on the bit lines.

10. The semiconductor device of claim 7, wherein the third insulating film patterns on the sidewalls of the bit lines are self-aligned relative to the contact spacers.

20

11. The semiconductor device of claim 7, wherein the contact patterns are wider than the bit lines.

12. The semiconductor device of claim 7, wherein the contact pattern and the
25 contact spacer comprise materials having etching selectivities relative to the third insulating film pattern.

13. The semiconductor device of claim 12, wherein the contact pattern and the contact spacer comprise silicon nitride or polysilicon.

30

14. The semiconductor device of claim 7, further comprising storage node contact plugs formed in the storage node contact holes and connected to the capacitor contact regions wherein the storage node contact plugs are formed using a second conductive film.

15. The semiconductor device of claim 14, wherein the storage node contact plugs are planarized when surfaces of the contact patterns are exposed.

16. The semiconductor device of claim 14, wherein the third insulating film patterns are continuously formed on surfaces and sidewalls of the bit lines, and the storage node contact plugs are planarized until surfaces of the third insulating film patterns are exposed.

17. A method of manufacturing a semiconductor device comprising:
forming a first insulating film on a semiconductor substrate;
forming wiring on the first insulating film wherein the wiring includes conductive film patterns and second insulating film patterns formed on the conductive film patterns;
forming a third insulating film on the wiring and the first insulating film using a silicon oxide based material;
forming contact patterns on the wiring wherein the contact patterns define contact hole regions;
forming contact spacers on sidewalls of the contact patterns; and
etching the third insulating film and the first insulating film using the contact patterns and the contact spacers as masks to form the contact holes and to simultaneously form third insulating film patterns on sidewalls of the wiring.

18. The method of claim 17, further comprising planarizing a predetermined portion of the third insulating film positioned on the wiring before forming the contact patterns.

19. The method of claim 17, further comprising planarizing the third insulating film until a surface of the second insulating film pattern is exposed before forming the contact patterns.

20. The method of claim 17, wherein the contact pattern is formed to have a sufficient thickness to protect the third insulating film during the etching process for forming the contact holes.

21. The method of claim 17, wherein the contact patterns are wider than the wiring.

22. The method of claim 17, wherein the contact spacer has a sufficient thickness to overlap a portion of the first insulating film.

23. The method of claim 17, wherein the contact pattern and the contact spacer
5 comprise materials having etching selectivities relative to the third insulating film.

24. The method of claim 23, wherein the contact pattern and the contact spacer comprise silicon nitride or polysilicon.

10 25. A method of manufacturing a semiconductor device comprising:
forming a first insulating film on a semiconductor substrate having capacitor contact regions;
forming bit lines on the first insulating film between the capacitor contact regions wherein the bit lines include first conductive film patterns and second insulating film patterns
15 formed on the first conductive film pattern;
forming a third insulating film on the bit lines and on the first insulating film wherein the third insulating film includes a silicon oxide based material;
forming contact patterns on the bit lines wherein the contact patterns define storage node contact hole regions;
20 forming contact spacers on sidewalls of the contact patterns; and
etching the third insulating film and the first insulating film using the contact patterns and the contact spacers as masks to form the storage node contact holes and to simultaneously form third insulating film patterns on sidewalls of the bit lines.

25 26. The method of claim 25, further comprising planarizing a predetermined portion of the third insulating film positioned on the bit lines before forming the contact patterns.

27. The method of claim 25, further comprising planarizing the third insulating film
30 until surfaces of the second insulating film patterns are exposed before forming the contact patterns.

28. The method of claim 25, wherein the contact pattern has a sufficient thickness to protect the third insulating film during an etching process for forming the storage node contact holes.

5 29. The method of claim 25, wherein the contact patterns are wider than the bit lines.

30. The method of claim 25, wherein the contact spacer has a sufficient thickness to overlap the capacitor contact region.

10 31. The method of claim 25, wherein the contact pattern and the contact spacer comprise materials having etching selectivities relative to the third insulating film.

15 32. The method of claim 31, wherein the contact pattern and the contact spacer comprise silicon nitride or polysilicon.

33. The method of claim 25, after forming the storage node contact holes, further comprising:

20 forming a second conductive film on the contact patterns, the contact spacers and the storage node contact holes wherein the second conductive film fills up the storage node contact holes; and

planarizing the second conductive film by a chemical mechanical polishing (CMP) process or an etch-back process to form storage node contact plugs in the storage node contact holes wherein the storage node contact plugs are connected to the capacitor contact regions.

25 34. The method of claim 33, wherein the second conductive film is planarized when surfaces of the contact patterns are exposed.

30 35. The method of claim 33, further comprising planarizing a predetermined portion of the third insulating film positioned on the bit lines before forming the contact patterns; and

planarizing the second conductive film until surfaces of the third insulating film patterns formed on the bit line are exposed.

36. The method of claim 35, wherein the third insulating film pattern has a sufficient thickness to protect the bit lines.

37. A semiconductor device comprising,
5 a semiconductor substrate;
a first insulating film on the substrate;
conductive film patterns having sidewalls, and a second insulating film on the first insulating film; and

10 a third insulating film including a silicon-oxide-based material on sidewalls of the wiring, the third insulating film defining contact hole regions, the contact holes passing through the first insulating film,

whereby a parasitic capacitance between the wiring can be reduced because the silicon oxide on the sidewalls of the wiring has a low dielectric constant.

15 38. A DRAM memory device including in combination:
a semiconductor substrate;
a plurality of bit-lines, the bit lines having silicon oxide spacers between the bit lines;
and

20 gate electrodes for word lines, the gate electrodes including a gate insulating film, a gate capping film including silicon nitride and a gate sidewall spacer including silicon nitride.